Digital Circuits

1 Introduction

1.1 Logic gate circuits

In computers, instruments, and control automatons, circuits that express certain logical relationships play a fundamental role. The building blocks of these logical circuits are the so-called logic gates. A logic gate can exist in two possible states: an open and a closed state, which correspond to the logical “yes” (true) and “no” (false). The simplest circuit element with two possible states is the single-pole switch, which conducts current when closed and does not conduct when open.

An integrated circuit in this context is a very small-sized circuit formed on a semiconductor chip (or possibly multiple chips). A typical component of an integrated circuit is the integrated transistor, which may be either a bipolar transistor or a MOS transistor. Accordingly, we distinguish between TTL (Transistor-Transistor Logic) and CMOS (Complementary Metal-Oxide Semiconductor) integrated circuits.

Logical relation		Truth table			Symbol	
Alg.	Operation	A	B	F	US.	INT.
A•B	AND	0 0 1 1	0 1 0 1	0 0 0 1		
A+B	OR	0 0 1 1	0 1 0 1	0 1 1 1		
$\overline{A}$	NOT	0 1		1 0		
$\overline{A \cdot B}$	NAND	0 0 1 1	0 1 0 1	1 1 1 0		
$\overline{A+B}$	NOR	0 0 1 1	0 1 0 1	1 0 0 0		
A⊕B	XOR	0 0 1 1	0 1 0 1	0 1 1 0		
$\overline{A \oplus B}$	XNOR	0 0 1 1	0 1 0 1	1 0 0 1		

Figure 1: Logic gate symbols and truth tables

When designing logic circuits, our goal is that upon the occurrence of certain events, the circuit controls a device in a predetermined manner. For example, an elevator should start moving upward if a button corresponding to a higher floor is pressed inside the cabin, or if the elevator is standing at a floor and the call button is pressed on an upper floor—but it must not start if the door is open, etc. Here we are dealing with the occurrence or non-occurrence

of certain possible events, and with the responses to these event combinations (in our case: whether the elevator moves upward, downward, or remains stationary).

Events that either occur or do not occur, and the statements or propositions referring to their occurrence—which can be true or false—can be regarded as logical variables, i.e., variables that can take two possible values: 1 and 0. The value of a logical variable is 1 if the event occurs (if the statement is true), and 0 otherwise.

Events can also be illustrated using switches: turning the switch on represents the occurrence of the event, while the off state indicates that the event has not occurred.

Integrated circuits within a given package may be arranged, for instance, in the following way.

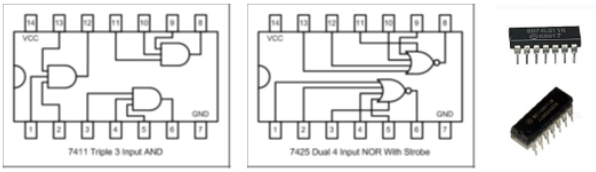

Figure 2: Possible packaging and pin configuration of logic gates

Since computer and control engineering devices can fundamentally be regarded as sequential networks, these have great significance. Sequential networks also contain combinational logic networks. The common part of synchronous and asynchronous networks is the combinational network, which generates the control functions of the storage elements by utilizing the output states.

1.2 Sequential networks

The task of sequential networks, also known as sequential circuits, is the implementation of time-dependent logic functions. An important property is that the output states are influenced not only by the input conditions but also by the previously occurring output events. Two major categories of sequential networks are distinguished:

- Asynchronous sequential networks
- Synchronous sequential networks

1.2.1 Asynchronous networks

A sequential network in which the dependence on the previous output state is realized by feedback or by storage elements. The output characteristic responds immediately to a change in the input characteristic.

1.2.2 Synchronous networks

The state transition takes place under the effect of an enabling signal, in the same phase as that signal. This enabling signal is called the clock signal. The dependence on the previous output state is realized by means of storage elements.

1.2.2.1. The role of the clock signal

With the help of a clock signal, it is possible to control the operation of two or more networks in the same timing. The memory stores the signals characteristic of the network state during the given clock period.

1.2.3 Types of integrated storage circuits

Flip-flops are the most important storage elements of digital circuits. In technical terminology, they are also called bistable multivibrators, or simply bistable circuits.

They have two fundamental properties:

- They possess two opposite states, either of which can be maintained without external intervention.
- They are provided with one or more inputs, through which the circuit can be switched from one state to the other.

A bistable circuit is capable of storing one bit of information! (basic memory element, RAM cell)

1.2.3.1. RS-type flip flop

S	R	Q^{n+1}
0	0	Q^n
0	1	0
1	0	1
1	1	x

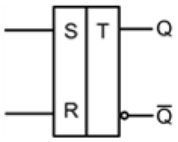

Figure 3: Truth table and circuit symbol of the RS-type flip-flop

It has two inputs (S and R) and two outputs (Q and $\bar{Q}$). In the table, Q^n denotes the current state, while Q^{n+1} denotes the state after control. S (set) is the write input through which the information to be stored can be written. R (reset) is the input through which the stored information can be cleared.

For such storage elements, the input combination S=1 and R=1 is forbidden, since writing and clearing at the same time is meaningless. The combination network that forms the storage element will switch randomly into one of the states.

1.2.3.2. JK-type flip flop

It eliminates the forbidden input combination of the RS flip-flop. (J: set input, K: reset input).

J	K	Q^{n+1}
0	0	Q^n
0	1	0
1	0	1
1	1	$\overline{Q^n}$

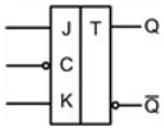

Figure 4: Truth table and circuit symbol of the JK-type flip-flop

1.2.3.3. T-type flip flop

We obtain a T flip-flop if the inputs of a JK flip-flop are connected together, that is, those value combinations are excluded when J and K are not equal. It has one data input and one control input.

T	Q^{n+1}
0	Q^n
1	$\overline{Q^n}$

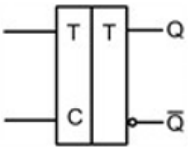

Figure 5: Truth table and circuit symbol of the T-type flip-flop

1.2.3.4. D-type flip flop

The information applied to its input appears at the output delayed by the duration of a control signal. We obtain a D flip-flop if the J=K value combinations are excluded.

D	Q^{n+1}
0	0
1	1

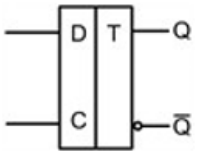

Figure 6: Truth table and circuit symbol of the D-type flip-flop

1.2.4 In general about storage elements

The state and state transitions of storage elements can be influenced not only by the input logic combinations but also by the clock signal. Accordingly, storage circuits can be classified as follows:

- Static storage elements
- Static gated storage elements
- Two-stage storage elements
- Edge-triggered storage elements

If information is applied to the input of static storage elements, the logical value of the output changes immediately. The disadvantage of this is that even a non-useful signal at the input (a random signal, e.g., noise) also causes a state change at the output.

The RS flip-flop is the simplest asynchronous sequential network. Its characteristic feature is that its output state changes instantaneously, in a bistable manner, under the effect of an input signal combination. This property makes it unsuitable for constructing synchronous sequential networks.

The clock signal, also called the gating signal, eliminates the effect of random signals applied to the input. The state of a controlled flip-flop can only change in synchronism with the C clock signal.

In certain circuits, it is necessary that the flip-flop not only operates in synchronism with the clock but can also be controlled at any time. Such storage circuits are provided with direct set and direct reset inputs.

1.2.5 Counter circuits

Counter circuits are important functional units of sequential networks. Their task is to record and indicate—that is, to count—the number of pulses arriving at their input. In principle, any circuit can be considered a counter circuit if—within certain limits—there is a clear relationship between the number of received pulses and the state of the output variables.

Thus, counting is based on two well-distinguishable operations:

- storage
- addition

Counter circuits must store the result of the pulse count and modify it appropriately upon the arrival of a new pulse. Therefore, a counter circuit must have at least as many distinct states as the maximum number of pulses to be counted. When the counter reaches the largest storable number, it restarts the counting from the beginning.

While the basic circuit of registers is the D flip-flop (a typical RAM cell), the most typical basic circuit of counter circuits is considered to be the T flip-flop. However, using JK flip-flops as the basic circuit provides greater flexibility in implementing special logic functions.

To determine the number of flip-flops required to build a counter, one must note that one flip-flop is needed for storing each bit. A four-bit counter therefore contains 4 flip-flops and can count up to a maximum of 15, which, including the zero value, means 16 distinct numbers.

Let us examine a 1-bit counter built with a T flip-flop and its timing diagram. (The T flip-flop is constructed from a JK flip-flop.) It can be observed that the T flip-flop toggles to the opposite state with every clock (CLK) pulse. Since it has two distinguishable states, it is suitable only for unambiguously counting two clock pulses. To count more than two pulses, naturally more than two distinct states are required, which can be achieved by increasing the number of flip-flops used in the counter.

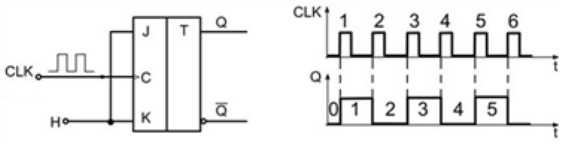

Figure 7: 1-bit counter circuit and timing diagram

1.2.5.1. Classification of counter circuits

There are many types of counter circuits; therefore, their classification can be done according to various criteria. Let us examine the most important classification aspects!

Based on the operation of the flip-flops forming the counter, we distinguish:

- **Asynchronous counters:** the clock signals generally drive only one flip-flop of the counter, usually the one representing the least significant bit. The other flip-flops receive their triggering signals from each other, toggling one another, so their transitions do not occur at the same instant. In other words, the operation is asynchronous.
- **Synchronous counters:** the clock signals simultaneously drive all the flip-flops forming the counter, and the state transitions are determined by a combinational network controlled by the previous values of the flip-flops. In this case, all flip-flops toggle at the same instant, meaning the operation is synchronous.

Based on the counting system (the number representation of the counter), we distinguish counters operating with different coding schemes:

- **Binary counter:** the stored pulse count is encoded in the binary number system;
- **Decimal counter:** the stored pulse count is encoded in the decimal number system;
- **Gray code counter:** the stored pulse count is encoded in Gray code;
- **Johnson counter:** the stored pulse count is encoded in Johnson code;
- **etc.**

Based on the counting direction (sequence), we distinguish:

- **Up counter:** the stored pulse count increases in ascending order, that is, with each incoming pulse it increases by one;
- **Down counter:** the stored pulse count decreases in descending order, that is, with each incoming pulse it decreases by one;
- **Up-down counter (reversible counter):** the counting direction can be reversed.

Pure down counters are not typically implemented in circuit form (in integrated circuits); usually, up-down counters are applied for realizing countdown functionality.

1.2.5.2. 4-bit asynchronous binary counter

If multiple T or JK flip-flops are connected in series, and the clock (CLK) input of each is connected to the output of the preceding flip-flop, we obtain an asynchronous binary counter circuit. To achieve up-counting, a negative edge-triggered flip-flop is used (with the condition J=K=1), so the output state of the flip-flop changes when the clock signal transitions from 1 to 0 (on the H–L edge). The counter can be expanded as desired using the RCO (Ripple Carry Output) terminal; for example, with 10 flip-flops it can count up to 1023. Asynchronous binary counters have a simple structure, but their operation is slow, since the propagation delays of the flip-flops add up.

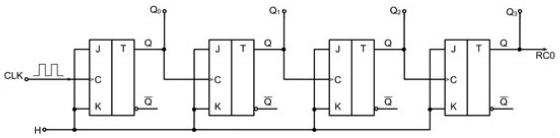

Figure 8: Circuit diagram of a 4-bit asynchronous binary counter

The disadvantage of asynchronous counters is that, in the worst case (when all outputs change state), the correct count result appears at the outputs only after all the flip-flops have toggled. This reduces the upper limit of the countable frequency, since at speeds exceeding a certain threshold the counter state may be incorrect. Therefore, asynchronous counters are not suitable for counting high-frequency pulses. The delay problems can be eliminated by using synchronous counters.

1.2.5.3. Synchronous binary counters

In synchronous counters, the clock inputs of all flip-flops are connected together, so the pulses to be counted drive all the flip-flops of the counter in synchronism, meaning that their toggling occurs simultaneously. In synchronous counters, the state transition is determined by the control applied to the logic inputs of the storage elements—usually JK or T flip-flops. This control can be realized, after appropriate design, by using the output signals and a combinational logic network.

In synchronous binary counters, during up-counting a given flip-flop toggles when all flip-flops representing lower-order bits store a logic 1. This condition can be checked with AND gates.

Let us analyze the circuit diagram of a 4-bit synchronous binary up-counter built from positive edge-triggered T flip-flops. All flip-flops receive the same clock signal, which makes this type faster in operation, since its switching time equals the switching time of a single flip-flop. However, its structure is more complex, as in addition to the flip-flops, logic gates are also required to generate the control signals.

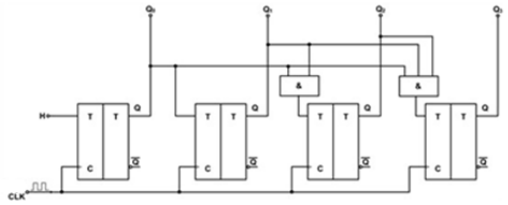

Figure 9: Circuit diagram of a synchronous binary counter

1.3 Output types of digital circuits

The output of digital circuits can generally be of three types. In the diagrams below, the output transistors are represented by switches.

1.3.1 Totem-pole output

Totem-pole outputs must not be connected together! They can produce only two states (L and H level). When opposite levels are driven, the resulting large currents may cause damage.

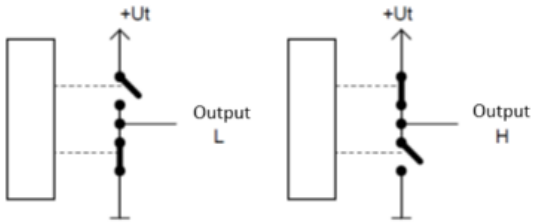

Figure 10: Schematic structure of a totem-pole output

1.3.2 Open-collector output

The L level is provided by an active semiconductor switch, while the H level is established by a resistor. The resistor is usually not built into the circuit! The L–H transition of an open-collector output is slower than that of a totem-pole output. Compared to the resistance of the switched-on semiconductor, the much higher resistance of the pull-up path causes the ever-present stray capacitances to charge relatively slowly.

Open-collector outputs can be connected together, enabling a wired-AND connection. If any OC output provides an L level, then the resulting output will also be L.

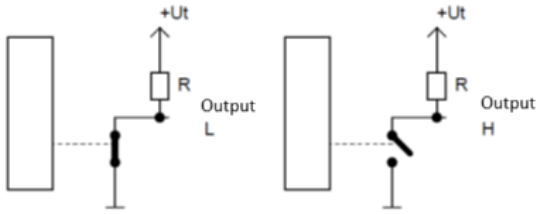

Figure 11: Schematic structure of an open-collector output

1.3.3 Three-state output

The L and H levels are provided by active semiconductor switches, but in the third state both are turned off. Circuits with three-state outputs can be connected together, provided that only one is active at a time. The Z state is called the high-impedance state.

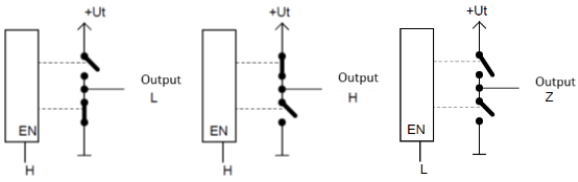

Figure 12: Schematic structure of a three-state output

1.4 Other parameters of digital circuits

The characteristics describing non-ideal behavior can be divided into two main groups:

- Dynamic (time-dependent) properties (e.g., propagation delay)
- Static properties (e.g., driving capability)

1.4.1 Propagation delay time (tpd)

The amount of delay of the output signal transition relative to the input signal transition. For different transition directions (H–L, L–H), the propagation delays may differ.

1.4.2 Rise and fall time

In real circuits, the rate of signal change is limited, so digital signals also have a finite slope. Rise time and fall time are defined as the time it takes for a signal transition to go from 10$\%$ to 90$\%$ of its final value (or vice versa).

1.4.3 Pulse width (t_W, pulse duration)

The pulse width is defined as the minimum width of the signal between its edges at the L and H levels. For the asynchronous clear and preset inputs of flip-flops, a minimum pulse width is specified. For the clock input of synchronous circuits, it is customary to specify the maximum clock frequency as well.

1.4.4 Setup time (t_{SU})

One signal must already be stable for a specified minimum time before the arrival of the next signal. Failure to meet this requirement is the source of the most serious problems.

1.4.5 Hold time (t_H)

One signal must not be changed for at least the specified time after the appearance of another signal (e.g., after the clock edge, the data at the flip-flop input must be held stable for this duration).

1.4.6 Supply voltages and logic levels

It depends on the logic circuit family, but typically a 5 V supply voltage is used. CMOS circuits, however, can operate over different supply voltage ranges.

Logic values are represented by voltage ranges; for example, a voltage below about 0.8 V is generally considered a low level, while a voltage above about 2.4 V is regarded as a high level when operating with a 5 V supply.

A small amount of noise superimposed on the input signal does not yet cause incorrect logic level detection.

1.4.7 Output drive capability

An unlimited number of logic inputs cannot be connected to a single logic output, since it can deliver only a finite current (a few mA). The number of standard gate inputs that can be connected to one output is called the fan-out.

2 Exercises

2.1 Examination of a logic gate (black-box measurement)

a) Apply a 5 V supply to the Vcc (pin 14) relative to GND (pin 7). Pins 1 and 2 are inputs, and their corresponding output is pin 3. These terminals belong to a two-input logic gate. There are 4 gates in the package. Record the gate's truth table by varying the input values (apply 0 V or 5 V to the inputs in the appropriate combinations). Examine the output using a multimeter. Write down the voltage levels corresponding to the low and high states that appear at the output. Based on the results, determine the type of the gate.

b) What gate do you obtain if you connect inputs 1 and 2 of the examined circuit together?

c) Using the gate constructed in task b), determine the gate's switching thresholds. Increase the input voltage from 0 V to 5 V in 0.1 V steps. Does the switching exhibit hysteresis?

d) Apply a 1 kHz square wave with a 0–5 V amplitude range to the circuit. Using an oscilloscope, determine the rise and fall times of the output signal as a function of the input signal.

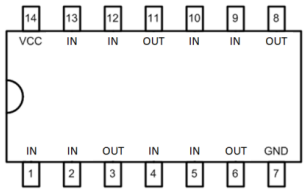

Figure 13: Logic gate package diagram

2.2 Examination of a BCD counter (SN74HCT390)

a) Assemble the circuit shown in Fig 14 (Pin 8 GND = 0 V, Pin 16 Vcc = 5 V)

b) Record the truth table of the circuit using a 1 Hz square wave with a 0–5 V range applied to the circuit input.

c) Using an oscilloscope, examine the individual outputs with respect to a 1 kHz input square wave frequency, and describe the operation.

d) Extend the circuit (Fig 15) with an SN7447 (Pin 8 GND = 0 V, Pin 16 Vcc = 5 V) and an HDSP-5731 seven-segment display. Test the circuit using a 1 Hz input square wave with a 0–5 V range, and describe your observations.

e) Modify the circuit with feedback and the gates used in Task 2.1 so that the counting resets at 6.

f) In the report, justify by calculation the value of the 270 Ω series resistors. Assume that a 5 V high level is expected at the counter output, the LED forward voltage is 1.8 V, and its current is 10 mA. What should be the minimum power rating of the resistor?

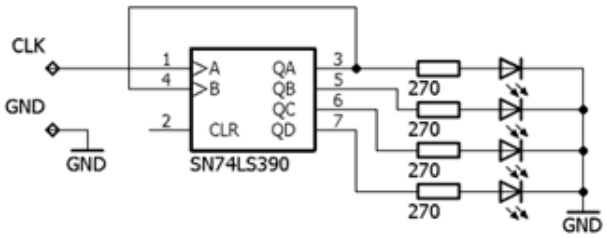

Figure 14: BCD counter

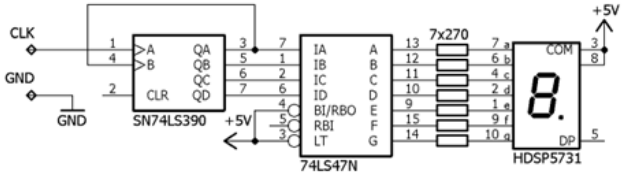

Figure 15: BCD counter with decoder and 7-segment display

Please include in the report a detailed list of all measuring instruments, generators, cables, and components used, specifying their types, model numbers, quantities, and values whenever available on the devices. Ensure that the photo sizes are optimized so that the report does not exceed 10 MB in total.

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